U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: SAIJO=7

U S APPLICATION NO (If known, see 37 CFR 1 5): 10/009196

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY CLAIMED
PCT/JP00/03746	09 June 2000	10 June 1999

TITLE OF INVENTION: CLAD PLATE FOR FORMING INTERPOSER FOR SEMICONDUCTOR DEVICE...

APPLICANT(S) FOR DO/EO/US: **Kinji SAIJO et al.**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S C. 371(b) and PCT Articles 22 and 39(1).
4. [X] The US has been elected in a Demand by the expiration of 19 months from the priority date (PCT Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not transmitted by the International Bureau).
   b. [X] has been communicated by the International Bureau
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. Amendments to the claims of the International Application under PCT Article 19 (35 U S.C 371(c)(3))
   [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   [ ] have been communicated by the International Bureau.
   [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   [X] have not been made and will not be made.
8. [ ] English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3))
9. [ ] Oath or declaration of the inventor(s) (35 U S.C. 371(c)(4)).
10. [ ] English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [X] Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3 31 is included
13. [X] A first preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items or information:
    [X] Courtesy copy of the first page of the International Publication (WO 00/77850)
    [X] Courtesy copy of the International Preliminary Examination Report (In Japanese). There were no annexes
    [X] Formal drawings, 5 sheets, Figures 1-12.
    [X] Courtesy Copy of the International Search Report
    [X] Application Data Sheet
    [X] The application is (or will be) assigned to: TOYO KOHAN CO., LTD., whose address is 2-12, Yonbancho, Chiyoda-ku, Tokyo 102-8447, Japan.

U.S. APPLICATION NO (If known, see 37 CFR 1 5)	International Application No	Attorney's Docket No
10/009196	PCT/JP00/03746	SAIJO=7

17. [xx] The following fees are submitted:

	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a)(1) –(5):	
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO..... .....**$1040.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO. **$890.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1 445(a)(2)) paid to USPTO.... .....**$740.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)... ....**$710.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)... ....**$100.00**	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [X] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$ 130.00	
Claims as Originally Presented	Number Filed	Number Extra	Rate		
Total Claims	7 - 20		X $18.00	$	
Independent Claims	3 - 3		X $84.00	$	
Multiple Dependent Claims (if applicable)			+$280.00	$ 280.00	
TOTAL OF ABOVE CALCULATIONS =				$1,300.00	
Claims After Post Filing Prel. Amend	Number Filed	Number Extra	Rate		
Total Claims	- 20		X $18.00	$	
Independent Claims	- 3		X $84.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1,300.00	
Reduction of ½ for filing by small entity, if applicable. Applicant claims small entity status. See 37 CFR 1.27				$	
SUBTOTAL =				$1,300.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
TOTAL NATIONAL FEE =				$1,300.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$1,300.00	
				Amount to be: refunded	$
				charged	$

a. [ ] A check in the amount of $_____ to cover the above fees is enclosed.
b. [X] Credit Card Payment Form (PTO-2038), authorizing payment in the amount of $ 1,300.00, is attached.
c. [ ] Please charge my Deposit Account No. **02-4035** in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.
d. [**XX**] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **02-4035**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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Date of this submission **December 10, 2001**

SIGNATURE

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REGISTRATION NUMBER

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY.'S DOCKET: SAIJO=7

In re Application of: Kinji SAIJO et al.	)	Art Unit:
	)	Examiner:
I.A. No.: PCT/JP00/03746	)	Washington, D.C.
Filed: June 9, 2000	)	December 10, 2001
For: CLAD PLATE FOR FORMING...	)	

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

Contemporaneous with the filing of this case, kindly amend as follows:

IN THE SPECIFICATION

After the title please insert the following paragraph:

--REFERENCE TO RELATED APPLICATIONS

The present application is the national stage under 35 U.S.C. §371 of international application PCT/JP00/03746, filed June 9, 2000 which designated the United States, and which application was not published in the English language.--

In re of: Kinji SAIJO et al. (SAIJO=7)

10/009196

JC10 Rec'd PCT/PTO 10 DEC 2001

REMARKS

The above amendment to the specification is being made to insert reference to the PCT application of which the present case is a U.S. national stage.

Favorable consideration is earnestly solicited.

Respectfully submitted,
BROWDY AND NEIMARK, P.L.L.C.
Attorneys for Applicant

By: ______________________
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Art Unit:
Kinji SAIJO et al	)	
IA No.: PCT/JP00/03746	)	Washington, D.C.
IA Filed: May 9, 2000	)	
U.S. App. No.: 10/009,196	)	**MONDAY**, April 15, 2002
National Filing Date: December 10, 2001	)	
For:	)	Docket No.: SAIJO=7

SUPPLEMENTAL AMENDMENT

Honorable Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to examination upon the merits, kindly amend as follows:

IN THE CLAIMS

Please amend claims 4 and 6 as follows:

4. (Amended) An interposer for use in a semiconductor device in which a clad plate as defined in any one of claims 1 or 2 is etched selectively to form connecting bumps with a semiconductor chip and a wiring layer, the semiconductor chip and the wiring layer are connected by way of the semiconductor chip connection bumps using anisotropically conductive adhesives and conduction of the interposer in the direction of the thickness is taken by way of a columnar conductor formed by etching.

6. (Amended) A method of manufacturing an interposer-forming clad layer for use in a semiconductor device as defined in any

one of claims 1 or 2 wherein the interposer-forming clad plate for use in the semiconductor device is formed by previously applying an activating treatment to the bonded surfaces of the copper foil and the nickel foil or nickel plating in a vacuum vessel and them laminating the copper foil and the nickel foil material or nickel plating and cold press-bonding them at a rolling reduction of 0.1 to 3% in which the activating treatment is applied <1> in an inert gas atmosphere at an extremely low pressure of 1 x 10^{1} to 1 x10^{-2} Pa, <2> using the nickel plated copper foil material and the copper foil material as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.

Please add claims 7 and 8 as follows:

7 (New).-- A method of manufacturing an interposer-forming clad layer for use in a semiconductor device as defined in claim 3 wherein the interposer-forming clad plate for use in the semiconductor device is formed by previously applying an activating treatment to the bonded surfaces of the copper foil and the nickel foil or nickel plating in a vacuum vessel and them laminating the copper foil and the nickel foil material or nickel plating and cold press-bonding them at a rolling reduction of 0.1 to 3% in which the activating treatment is applied <1> in an inert gas atmosphere at an extremely low pressure of 1 x 10^{1} to 1 x10^{-2} Pa, <2> using the nickel plated copper foil material and the copper foil material as one electrode A having the bonding surfaces grounded to the earth,

respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.--

8 (New).-- An interposer for use in a semiconductor device in which a clad plate as defined in claim 3 is etched selectively to form connecting bumps with a semiconductor chip and a wiring layer, the semiconductor chip and the wiring layer are connected by way of the semiconductor chip connection bumps using anisotropically conductive adhesives and conduction of the interposer in the direction of the thickness is taken by way of a columnar conductor formed by etching.--

If, inadvertently, a proper multiple dependent claim has not been amended to reduce it to single dependency, please amend it to be dependent solely on the first-mentioned claim, or, if that is not possible, please cancel the claim and notify the undersigned.

REMARKS

The above amendments to the claims are being made in order to eliminate multiple dependency and for the purpose of reducing the filing fee. Please enter this amendment prior to calculation of the filing fee in this case.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**."

In re of: SAIJO=7

Favorable consideration and allowance are earnestly solicited.

Respectfully submitted,
BROWDY AND NEIMARK, P.L.L.C.
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 4 and 6 have been amended as follows:

4 (Amended).--An interposer for use in a semiconductor device in which a clad plate as defined in any one of claims 1 [to 3] or 2 is etched selectively to form connecting bumps with a semiconductor chip and a wiring layer, the semiconductor chip and the wiring layer are connected by way of the semiconductor chip connection bumps using anisotropically conductive adhesives and conduction of the interposer in the direction of the thickness is taken by way of a columnar conductor formed by etching.--

6. (Amended).--A method of manufacturing an interposer-forming clad layer for use in a semiconductor device as defined in any one of claims 1 [to 3] or 2 wherein the interposer-forming clad plate for use in the semiconductor device is formed by previously applying an activating treatment to the bonded surfaces of the copper foil and the nickel foil or nickel plating in a vacuum vessel and them laminating the copper foil and the nickel foil material or nickel plating and cold press-bonding them at a rolling reduction of 0.1 to 3% in which the activating treatment is applied <1> in an inert gas atmosphere at an extremely low pressure of 1×10^{1} to 1×10^{-2} Pa, <2> using the nickel plated copper foil material and the copper foil material as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.--

[Name of document] SPECIFICATION

INTERPOSER-FORMING CLAD PLATE FOR USE IN SEMICONDUCTOR DEVICE, AN INTERPOSER FOR USE IN A SEMICONDUCTOR DEVICE AND A MANUFACTURING METHOD OF THEM

Technical Field

This invention concerns an interposer-forming clad plate for use in a semiconductor device which is a substrate to mount semiconductor chips, an interposer for use in a semiconductor device to be manufactured by using the clad material, as well as a manufacturing method of them.

Background of the Invention

In recent years, along with reduction of size and weight and enhancement for the function of electronic equipments, size reduction has been required also for semiconductor packaging devices mounted therein and small-sized package devices have been developed. Then, a semiconductor device of a size substantially equal with the chip size has been proposed. Japanese Patent Laid-Open No. 74807/1998 discloses a method of manufacturing such a semiconductor device and a schematic view thereof is shown in Fig. 12. A semiconductor chip 101 is mounted on one side of an interposer 100 (substrate) and connected with a wiring pattern 102 on the substrate. Further, the wirings are conducted through via

holes 103 formed in the direction of the thickness of the substrate to a mounting substrate, and solder bumps 104 for external connection are formed to the via holes on the side of the mounting substrate.

In the semiconductor device of the constitution as described above, conduction between both surfaces of the interposer is taken by forming through holes and then filling a conductive material, for example, by plating. However, steps of forming fine through holes and applying plating therein results in a technical difficulty and it requires to apply a relatively thick plating to bring about a problem of increasing the cost.

This invention intends to solve the subject described above and it is a subject thereof to provide an interposer-forming clad plate for use in a semiconductor device capable of being manufactured at a reduced cost and having favorable characteristics, an interposer for use in a semiconductor device using the same and a manufacturing method of them.

Disclosure of the Invention

An interposer-forming clad plate for use in a semiconductor device according to this invention has a feature that it is manufactured by press-bonding a copper foil material and a nickel foil material at a rolling reduction of 0.1 to 3%.

A clad plate according to this invention has a feature that it is manufactured by press-bonding a copper foil material having

nickel plating on one or both surfaces and another copper foil material or a copper foil material having a nickel plating on one surface at a rolling reduction of 0.1 to 3%.

Another feature of the clad plate according to this invention resides in that it consists of five layers of copper/nickel/copper/nickel/copper.

The interposer for use in the semiconductor device according to this invention is characterized in that one of the clad plates described above is selectively etched to form connection bumps with a semiconductor chip and wiring layers, the semiconductor chip and the wiring layer are connected through the semiconductor chip connection bumps by using anisotropically conductive adhesives and conduction in the direction of the thickness of the interposer is taken by way of a columnar conductor formed by etching.

A method of manufacturing a interposer for use in a semiconductor device according to this invention is characterized by laminating a copper foil material forming a conductor layer or the like, a nickel foil material or nickel plating forming an etching stop layer and press-bonding them at a rolling reduction of 0.1 to 3% to form a clad plate for forming an interposer for use in a semiconductor device, selectively etching the clad plate to form a columnar conductor, forming an insulation layer on a copper foil material forming a wiring layer, and forming semiconductor chip connection bumps and a wiring layer to the clad plate on the

side opposite to the columnar conductor forming surface.

A method of manufacturing a clad plate according to this invention is characterized by forming a clad plate by previously applying an activating treatment to a bonding surface of a copper foil and a nickel foil or nickel plating in a vacuum vessel, then laminating the copper foil and, the nickel foil or the nickel plating and cold press-bonding them at 0.1 t0 3% rolling reduction in which the activating treatment is conducted <1> in an inert gas atmosphere at an extremely low pressure of 1×10^{1} to 1×10^{-2} Pa, <2> using the nickel plated copper foil material and the copper foil material as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.

Brief Description of the Drawings

Fig. 1 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 2 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 3 is an explanatory view for the steps in a method of manufacturing an interposer for use in a

semiconductor device according to one embodiment of this invention. Fig. 4 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 5 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 6 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 7 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 8 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 9 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 10 is an explanatory view for the steps in a method of manufacturing an interposer for use in a semiconductor device according to one embodiment of this invention. Fig. 11 is a cross sectional front elevational view of an apparatus for manufacturing the clad plate. Fig. 12 is a cross sectional view of an existent interposer for use in a semiconductor device.

Best Mode for Carrying Out the Invention

This invention is to be explained concretely with reference to one embodiment shown in Fig. 1 to Fig. 10. At first, the structure of a semiconductor device according to one embodiment of this invention is to be explained with reference to Fig. 10.

As illustrated, etching stopper layers 11 and 12 (suitably with a thickness of 0.1 to 3 mm) are bonded on both surfaces of a wiring layer 10 comprising a copper foil (suitably with a thickness of 10 to 100 mm). A connection bump 18 (suitably with a thickness of 10 to 100 mm) for a semiconductor chip is formed at the top end of the wiring layer 10 on the side of mounting the semiconductor chip 1. Further, an insulative resin 13 is formed to the wiring layer on the side of the mounting substrate and conducted with the mounting surface is taken by way of a columnar conductor 17 (suitably with a thickness of 10 to 100 mm) and solder bumps 2 are formed on the mounting surface.

Then, explanation is to be made to a method of manufacturing an interposer for use in a semiconductor device described above. At first, nickel plating 20 and 21 as etching stopper layers 11 and 12 are applied on both surfaces of a copper foil 19 (suitably with a thickness of 10 to 100 mm) to form an internal conductor layer 10 upon manufacturing the interposer for use in the semiconductor device to manufacture a nickel plated copper foil material 22 (refer to Fig. 1).

Then, the nickel-plated copper foil material 22 is wound around a delivery reel 23 in a clad plate manufacturing apparatus

shown in Fig. 11. Further, a copper foil material 24 as a columnar contactor 17 is wound around a delivery reel 25. The nickel-plated copper foil material 22 and the copper foil material 24 are delivered simultaneously from the delivery reels 23 and 25 and a portion thereof is wound around electrode rolls 27 and 28 protruded in an etching chamber 26 and sputter etching is applied to activate in the etching chamber 26.

In the case, the activating treatment is applied as disclosed previously by the present applicant in Japanese Patent Laid-Open No. No. 224184/1989 <1> in an inert gas atmosphere at an extremely low pressure of 1×10^{1} to 1×10^{-2} Pa, <2> using the nickel plated copper foil material 22 and the copper foil material 24 as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.

Subsequently, they are cold press-bonded by a rolling unit 30 disposed in the vacuum vessel 29 and an interposer-forming clad plate 31 having three layered structure for use in a semiconductor device is wound around a delivery roll 32.

Then, the interposer-forming clad plate 31 for use in the semiconductor device having the three layered structure is again wound around the delivery roll 23. Further, a copper foil 33

(refer to Fig. 1) as a connection bump 18 is wound around the delivery reel 25. The clad plate 31 and the copper foil material 33 are unwound from the delivery reels 23 and 25 and a portion thereof is wound around the electrode rolls 27 and 28 protruded in the etching chamber 26 and applied with and activated by sputter etching treatment in the etching chamber 26.

Also in this case, the activating treatment is applied <1> in an inert gas atmosphere at an extremely low pressure of 1×10^{1} to 1×10^{-2} Pa, <2> using the nickel plated copper foil material 22 and the copper foil material 24 as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B to manufacture a clad plate 34 for use in the semiconductor device having a five layered structure.

In the foregoings, explanation has been made to an example of press-bonding a material formed by previously nickel plating on a copper foil material, a material formed by press-bonding a nickel foil to a copper foil material by using the apparatus described above may also be used instead of the nickel plating.

Further, by repeating the press-bonding using the apparatus described above, a multi-layered clad layer can be manufactured in which a copper layer is disposed to the surface and the rearface

layers and the nickel layer is interposed as the intermediate layer in the order of copper/nickel/copper/nickel/copper.

Further, when three or more sets of delivery reels are disposed, copper foil material or nickel foil material are disposed to the reels and foil materials are simultaneously supplied from the three or more reels, a clad plate of a multi-layered structure can be manufactured by press-bonding only for once.

After cutting the interposer-forming clad plate 34 for use in the semiconductor device into a desired size, an interposer for use in the semiconductor is manufactured by way of the following steps to be explained with reference to Fig. 2 to Fig. 9. At first, as shown in Fig. 2, after forming a photoresist film 35 on the surface of the copper foil 24, it is exposed and developed.

Then, as shown in Fig. 3, the copper foil material 24 is etched selectively and the copper foil 24 is removed leaving a columnar conductor 17. As an etching solution, sulfuric acid + aqueous hydrogen peroxide or ammonium persulfate liquid is used preferably.

Then, as shown in Fig. 4, the nickel layer 20 is removed by selective etching. As the etching liquid, it is desirable to use a commercially available Ni etching liquid (for example, Merstrip N-950, manufactured by Mertechs Co.) is used preferably.

Then, as shown in Fig. 5, an insulative resin 39 is coated. As the insulative resin 39, use of an epoxy or polyimide resin is

desirable.

Then, as shown in Fig. 6, polishing is applied to make the surface of the resin 39 uniform. In this case, the head of the columnar conductor 17 is exposed to the surface. Instead of the polishing, it is possible to chemically remove the resin on the columnar conductor to exposer the head.

Further, as shown in Fig. 7, the copper foil material 33 is etched selectively to remove the copper foil material 33 leaving the columnar conductor 18. As the etching liquid, it is preferred to use, for example, sulfuric acid + aqueous hydrogen peroxide or ammonium persulfate liquid.

Then, as shown in Fig. 8, the nickel layer 21 is removed. As the etching liquid, it is preferred to use a commercially available Ni etching liquid (for example Merstrip N-950, manufactured by Mertechs Co.).

Then, as shown in Fig. 9, a photoresist film 37 is formed on the surface of the copper foil material and exposed and developed to etch the copper foil 19 by using, for example, ferric chloride or sulfuric acid + aqueous hydrogen peroxide. Thus the wiring layer is formed.

As shown in Fig. 10, a semiconductor chip 1 is connected to the surface of a wiring layer by use of anisotropically conductive adhesives 4 containing conductive particles 3. Further, a solder bump 2 is formed at a position corresponding to the columnar conductor 17 on the side of the mounting substrate.

Industrial Applicability

As has been explained above, in the interposer-forming clad plate for use in the semiconductor device according to this invention, the copper foil material and the nickel foil material are press-bonded under a low rolling reduction of 0.1 to 3%, or the copper foil material having a nickel plating on one or both surfaces and other copper foil material or other copper foil material having a nickel plating on one or both surfaces in a laminated state are press-bonded at a low rolling reduction of 0.1 to 3%. Accordingly, the planarity at the bonding boundary can be maintained by suppressing the stress at the bonding boundary, and no alloyed metal is formed at the boundary since heat treatment for restoration of workability is no more necessary, it is possible to manufacture the interposer-forming clad plate for use in the semiconductor device of excellent selective etching property.

In the interposer for use in the semiconductor device according to this invention, since the interposer-forming clad plate for use in the semiconductor device as described above is etched selectively, to former connection bumps with semiconductor chip and the wiring layer and conduction of the interposer along the direction of the thickness is taken by way of the columnar conductor formed by etching, the interposer for use in the semiconductor device capable of coping with the small sized semiconductor device can be manufactured efficiently at a reduced

cost. Further, since connection between the semiconductor chip and the wiring layer is conducted through the semiconductor chip connection bumps by using anisotropically conductive adhesives containing conductive particles, there is no requirement for forming the bump on the semiconductor chip and the cost for the semiconductor device can be reduced.

In the method of manufacturing the interposer for use in the semiconductor device according to this invention, since the copper foil to form the conductor layer and the nickel plating to form the etching stopper layer are laminated and press-bonded to form the clad plate for use in the semiconductor device, the clad plate is etched selectively to form the columnar conductor, the insulation layer is formed on the copper foil material forming the wiring layer, and the bump and the wiring layer for connecting the semiconductor chip are formed to the clad plate on the side opposite to the columnar conductor forming surface, thereby manufacturing the interposer for use in the semiconductor device, the interposer for use in the semiconductor device capable of coping with a small sized semiconductor device can be manufactured efficiently and at a reduced cost.

In the method of manufacturing the interposer-forming clad plate for use in the semiconductor device according to this invention, since the clad plate is formed by previously applying the activating treat to the bonded surfaces of the copper foil and the nickel plating in the vacuum vessel, then laminating the

copper foil and the nickel plating and cold press-bonding them at a rolling reduction of 0.1 to 3% in a vacuum vessel, the planarity at the bonded boundary can be maintained by suppressing the stress at the bonding boundary, and since the heat treatment for the restoration of the workability is no more required and no alloy layer is formed at the boundary, the interposer-forming clad plate for use in the semiconductor device of excellent selective etching property can be manufactured.

CLAIMS

1. An interposer-forming clad plate for use in a semiconductor device manufactured by press-bonding a copper foil material and a nickel foil material at a rolling reduction of 0.1 to 3%.

2. An interposer-forming clad plate for use in a semiconductor device manufactured by press-bonding a copper foil material having nickel plating on one surface or both surfaces and other copper foil material or a copper foil material having nickel plating on one surface at a rolling reduction of 0.1 to 3%.

3. A clad plate as defined in claim 1 or 2, wherein the clad plate comprises five layers of copper/nickel/copper/nickel/copper.

4. An interposer for use in a semiconductor device in which a clad plate as defined in any one of claims 1 to 3 is etched selectively to form connecting bumps with a semiconductor chip and a wiring layer, the semiconductor chip and the wiring layer are connected by way of the semiconductor chip connection bumps using anisotropically conductive adhesives and conduction of the interposer in the direction of the thickness is taken by way of a columnar conductor formed by etching.

5. A method of manufacturing an interposer for use in a semiconductor device, which comprises laminating a copper foil material to form a conductor layer or the like and a nickel foil or nickel plating to form an etching stop layer, press-bonding them

at a rolling reduction of 0.1 to 3% to form an interposer-forming clad layer for use in a semiconductor device, selectively etching the clad plate to form a columnar conductor, forming an insulation layer on the copper foil material to form a wiring layer, and forming a semiconductor chip connection bumps and the wiring layer to the clad plate on the side opposite to the surface for forming the columnar conductor.

6. A method of manufacturing an interposer-forming clad layer for use in a semiconductor device as defined in any one of claims 1 to 3, wherein the interposer-forming clad plate for use in the semiconductor device is formed by previously applying an activating treatment to the bonded surfaces of the copper foil and the nickel foil or nickel plating in a vacuum vessel and then laminating the copper foil and the nickel foil material or nickel plating and cold press-bonding them at a rolling reduction of 0.1 to 3% in which the activating treatment is applied <1> in an inert gas atmosphere at an extremely low pressure of 1×10^{1} to 1×10^{-2} Pa, <2> using the nickel plated copper foil material and the copper foil material as one electrode A having the bonding surfaces grounded to the earth, respectively, and conducting glow discharge by applying an AC current at 1 to 50 MHz between it and the other electrode B supported insulatively and <4> applying sputter etching, <3> with the area of the electrode exposed in plasmas caused by the glow discharge being 1/3 or less of the electrode B.

[Name of document] ABSTRACT

A clad plate for forming an interposer for a semiconductor device which can be manufactured at low cost and has good characteristics, an interposer for a semiconductor device, and a method of manufacturing them. Copper foil materials (19, 24, 33) forming conductive layers (10, 17, 18) and nickel plating (20, 21) forming etching stopper layers (11, 12) are formed and pressed to form a clad plate (34) for forming an interposer for a semiconductor device. Thus, a clad plate (34) for forming an interposer for a semiconductor device is manufactured. The clad plate (34) is selectively etched to form a columnar (17) columnar conductor (17), and an insulating layer (13) is formed on the copper foil material forming a wiring layer (10). A bump (18) for connection of a semiconductor chip and the wiring layer (10) are formed on the opposite side to the side on which the columnar conductor (17) is formed. Thus, an interposer for a semiconductor device ia manufactured.

Fig. 1

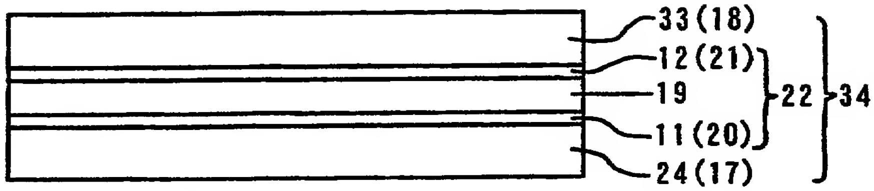


Fig. 2

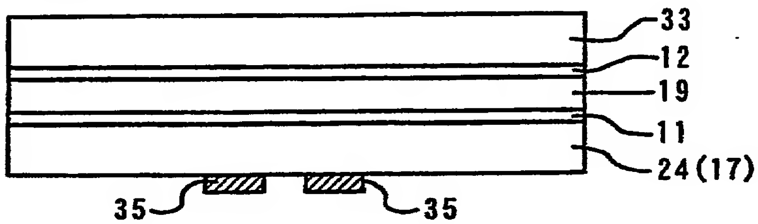


Fig. 3

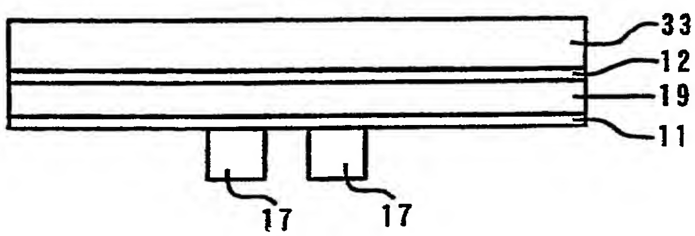


Fig. 4

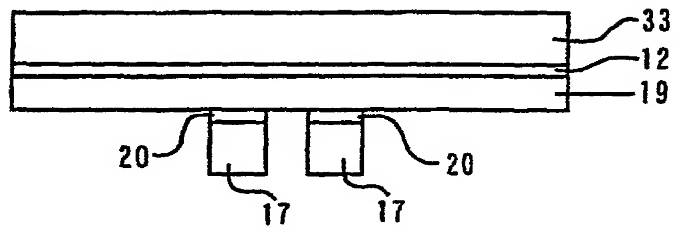


Fig. 5

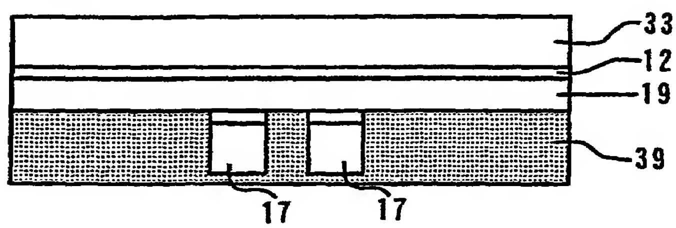


Fig. 6

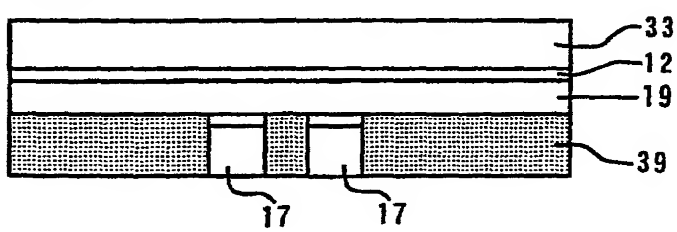


Fig. 7

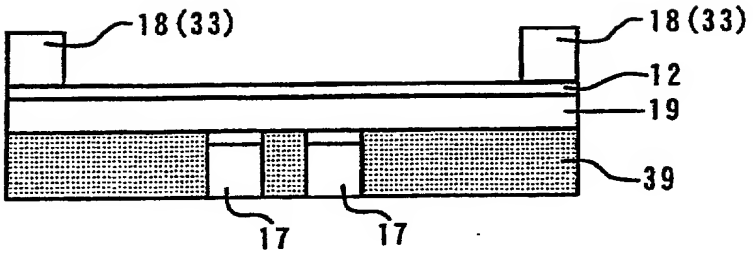


Fig. 8

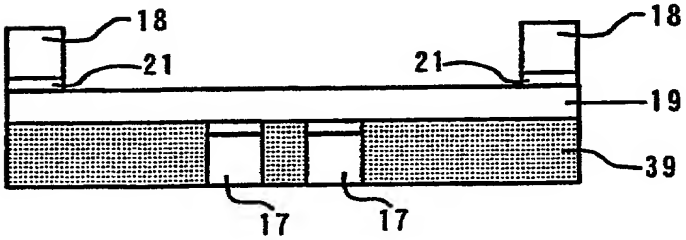


Fig. 9

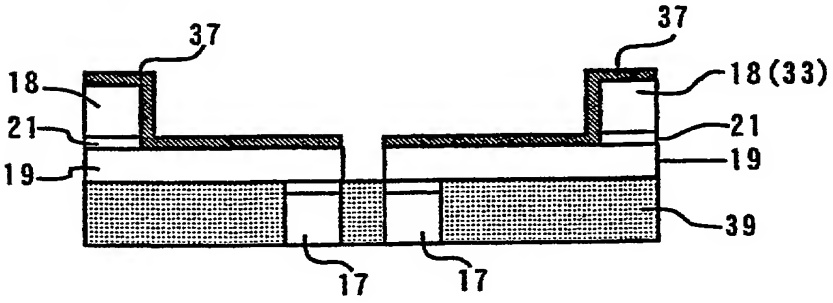


Fig. 10

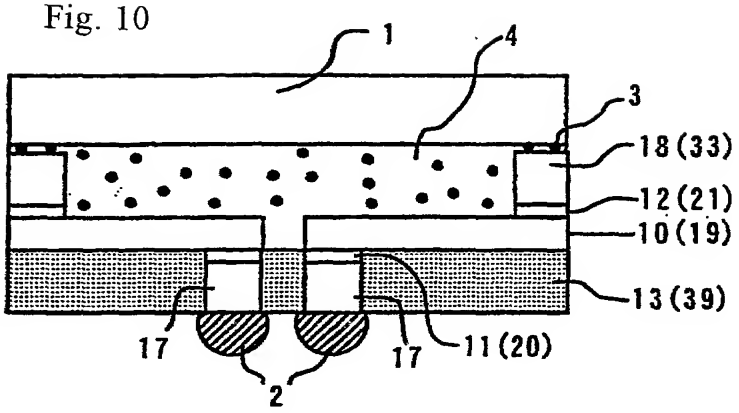


Fig. 11

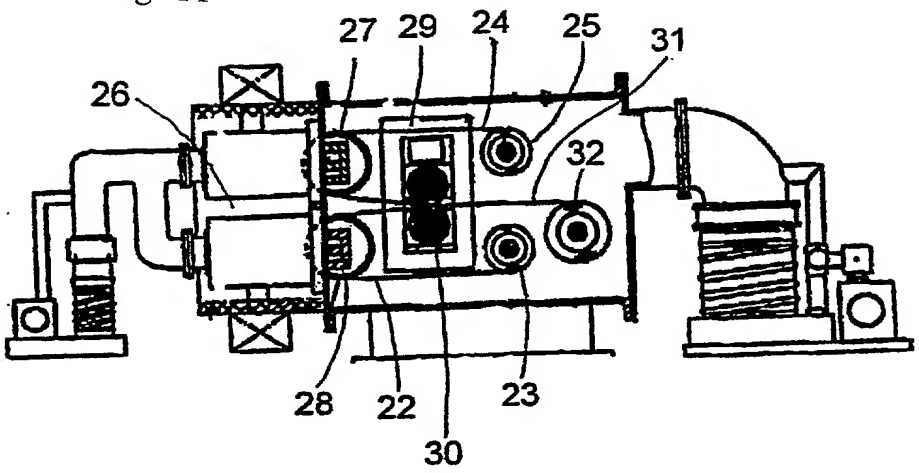
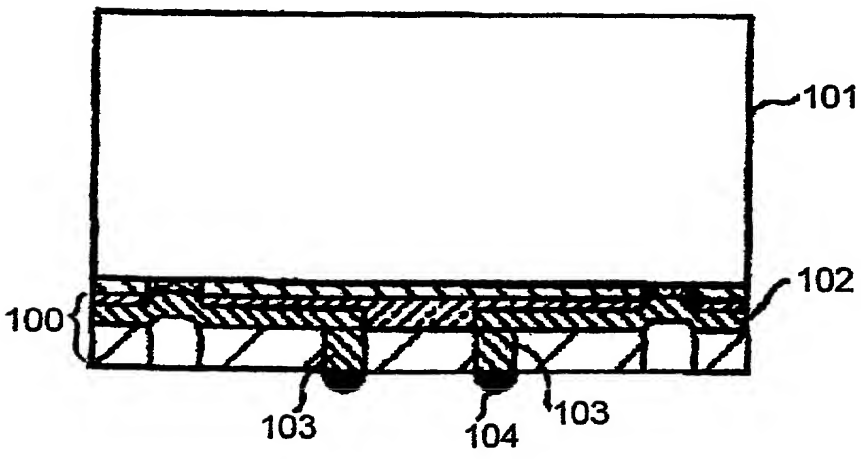


Fig. 12



Page 1 of 2 Pages [X] Original [ ] Substitute [ ] Supplemental Atty. Docket: SALJO=7

Combined Declaration for Patent Application and Power of Attorney

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CLAD PLATE FOR FORMING INTERPOSER FOR SEMICONDUCTOR DEVICE, INTERPOSER FOR SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THEM

the specification of which (check one)

[ ] is attached hereto;
[ ] was filed in the United States under 35 U.S.C. §111 on , as U.S. Appln. No. *; or
[X] was/will be filed in the U.S. under 35 U.S.C. §371 by entry into the U.S. national stage of an international (PCT) application, PCT/JP00/03746; filed June 9, 2000, entry requested on _____*; national stage application received U.S. Appln. No. _____*; §371/§102(e) date _____* (* if known)

and was amended on (if applicable).

(include dates of amendments under PCT Art. 19 and 34 if PCT)

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; and I acknowledge the duty to disclose to the Patent and Trademark Office (PTO) all information known by me to be material to patentability as defined in 37 C.F.R. §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119 (a)-(d) and 365 (b) of any prior foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or under §365(a) of any PCT application which designated at least one country other than the U.S., listed below:

Application No.	Country	Filing Date (MM/DD/YYYY)
11/164,454	JAPAN	06-10-1999

If I claimed foreign priority above, I hereby identify below any foreign application for patent (including an international (PCT) application designating a country other than the United States) or for an inventor's or plant breeder's certificate, having a filing date before that of the earliest application from which foreign priority is claimed (if left blank, then there are none):

Non-Priority Application No.	Country	Filing Date (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional applications listed below:

Application No.	Filing Date (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. §120 of any prior U.S. non-provisional application(s) or under §365(c) of any prior PCT international application(s) designating the U.S., listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in such U.S. or PCT international application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose to the PTO all information which is material to patentability as defined in 37 C.F.R. §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Filing Date (MM/DD/YYYY)	Status (patented, pending, abandoned)

As a named inventor, I hereby appoint the following registered practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Title: CLAD PLATE FOR FORMING INTERPOSER FOR SEMICONDUCTOR DEVICE, INTERPOSER FOR SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THEM

U.S. Application filed December 10, 2001, Serial No. 10/009,196
PCT Application filed May 9, 20000, Serial No. PCT/JP00/03746

The undersigned hereby authorizes the U.S. Attorneys or Agents appointed herein to accept and follow instructions from TOYO KOHAN CO., LTD. as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. Attorneys or Agents and the undersigned. In the event of a change of the persons from whom instructions may be taken, the U.S. Attorneys or Agents appointed herein will be so notified by the undersigned.

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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RESIDENCE		CITIZENSHIP
POST OFFICE ADDRESS		